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forming a p transistor and an n transistor in the heterostructure, wherein the strained layer comprises a channel of at least one of the transistors, the transistors being interconnected in a CMOS circuit.

The method of claim 32 wherein the heterostructure further comprises an insulating layer below the strained layer.

The method of claim wherein the heterostructure further comprises a SiGe graded buffer layer positioned between the relaxed Si<sub>1-x</sub>Ge<sub>x</sub> layer and the Si substrate.

The method of claim 21 wherein the strained layer comprises Si.

9 36. The method of claim 32 wherein 0.1 < x < 0.5.

The method of claim 22 wherein the CMOS circuit comprises a logic gate.

The method of claim 37 wherein the logic gate is a NOR gate.